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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/435,154	11/08/99	YAMAZAKI S	SEL142

MMC2/0925

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EXAMINER
LOKE,S

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/435,154	Yamazaki et al.
Examiner	**Art Unit**
Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 23, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-26* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892) 0

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 16

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

1. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 6, 14, 19, it is unclear whether a portion of the second conductive layer partially overlaps the first impurity region.

In claims 1, 6, 14, 19, it is unclear whether another portion of the second conductive layer partially overlaps the third impurity region.

In claims 11, 24, it is unclear whether the first gate electrode partially overlaps the first impurity region.

In claims 11, 24, it is unclear whether the second gate electrode partially overlaps the third impurity region.

In claims 6, 19, it is unclear whether the second conductive layer does not overlap the second impurity region.

In claim 12, lines 1-2, claim 25, lines 1-2, "said first and second gate electrode" is unclear whether it is being referred to "said first and second gate electrodes".

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al.

Miyasaka et al. discloses a LDD-type CMOS TFT circuits formed in a LCD device in figs. 26, 49A, 49B. It comprises: an n-channel TFT having LDD regions [9] and source and drain regions [3], a gate electrode [6] partially overlaps the LDD regions [9]; a p-channel TFT having LDD regions [10] and source and drain regions [4], a gate electrode [6] partially overlaps the LDD regions [10]; a wiring [8] is electrically connected to the p-type region [10].

It would have been obvious for the LCD device is a ferroelectric LCD device because it is a widely used liquid crystal material.

In regards to claim 12, it would have been obvious to have the claimed materials for the first and second gate electrodes because they are low resistance gate metal materials.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. in view of Kondo.

Miyasaka et al. differs from the claimed invention by not showing the gate electrode having a first conductive layer and a second conductive layer.

Kondo discloses a gate electrode having a first conductive layer (polysilicon) [4] and a second conductive layer (titanium silicide) [20] being in contact with a gate insulating film [3] and a top surface and side surfaces of the first conductive layer in fig. 1. The second conductive layer [20] partially overlaps the n-type LDD region [6a].

Since both Miyasaka et al. and Kondo teach a gate electrode overlaps the LDD region in a MOSFET, it would have been obvious to have the gate electrode structure of Kondo in each of the TFTs of Miyasaka et al. because it relaxes a concentration of an electric field at the end of the drain.

In regards to claims 2, 7, it would have been obvious to have the claimed materials for the first conductive layers of the MOSFETs because they are low resistance gate metal materials.

5. Claims 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. in view of Kondo, further in view of Johnson.

Miyasaka et al. and Kondo differ from the claimed invention by not showing the CMOS circuit is used in a goggle type display device.

Johnson shows a goggle type LCD display device having a control circuitry and a display screen [12] in figs. 1 and 2.

Since Miyasaka et al. and Johnson teach a LCD device with control circuitry, it would have been obvious to have the CMOS circuit of Miyasaka et al. in the control circuit of Johnson because it increases the speed of the device.

In regards to claims 15, 20, it would have been obvious to have the claimed materials for the first conductive layers of the MOSFETs because they are low resistance gate metal materials.

6. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. in view of Johnson.

Miyasaka et al. differs from the claimed invention by not showing the CMOS circuit is used in a goggle type display device.

Johnson shows a goggle type LCD display device having a control circuitry and a display screen [12] in figs. 1 and 2.

Since Miyasaka et al. and Johnson teach a LCD device with control circuitry, it would have been obvious to have the CMOS circuit of Miyasaka et al. in the control circuit of Johnson because it increases the speed of the device.

In regards to claim 25, it would have been obvious to have the claimed materials for the first and second gate electrodes of the MOSFETs because they are low resistance gate metal materials.

7. Applicant's arguments filed 7/23/01 have been fully considered but they are not persuasive.

It is urged, in pages 7-8 of the remarks, that the languages of claims 1, 6, 11, 14, 19 and 24 are clear and definite. However, it is important to note that the term "overlap" means "to lie or extend over and cover part of". Therefore, it is the second conductive layer overlaps the impurity region of each of the TFTs and it is not the impurity region overlaps the second conductive layer of each of the TFTs.

It is urged, in pages 8-10 of the remarks, that Miyasaka et al. never discloses a wiring is electrically connected to the third impurity region. However, the wiring [8] of Miyasaka et al. is electrically connected to the third impurity region [10] through the impurity region [4].

8. The substitute specification filed on 5/2/01 is acceptable.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920.

sl

September 22, 2001

Steven Loke
Primary Examiner

Steven Loke